# MPX 100 Dual Channel Processor

**Stereo 44.1kHz S/PDIF Digital Output**

*Service Manual*

lexicon

## SAFETY SUMMARY

**The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions, or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.**

### DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

### KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

### DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

### SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

**CAUTION**

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

**NOTE:**

The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.

**CAUTION**

### Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti-static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use anti-static containers for handling and transport.

*To make a plastic-laminated workbench anti-static, wash with a solution of liquid detergent, and allow to dry without rinsing.



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# 1 Controls and Connectors

## The Front Panel

**Bypass**
Mutes or bypasses the signal depending on the setting of the System Bypass parameter. (Press for 2 seconds to access System Parameters.)

**Adjust**
Modifies the parameters of the current program.

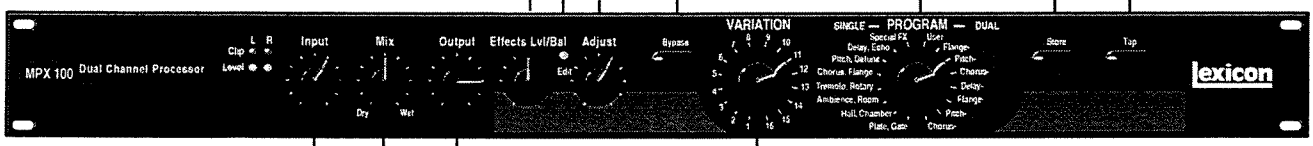
**Store**
Initiates store procedure. (When pressed with **Tap**, activates MIDI Learn.)

**TAP**
Flashes for tempo-based programs. Press twice to set a tempo. Hold to have input level determine tempo. (When pressed with **Store** activates MIDI Learn.)

**Edit LED**
Lights to indicate program is altered but not stored.

**Effects Lvl/Bal**
Sets the level of the Single effects and the balance of the Dual effects.

**PROGRAM**
Selects program banks (Single, Dual, or User).




**Input**
Sets the level of the incoming signal. LEDs indicate acceptable signal level (green), or clipping (red).

**Output**
Controls the analog output level.

**Mix**
Controls the proportion of processed (wet) to unprocessed (dry) signals.

**VARIATION**
Selects program variations for the effect bank currently selected by the PROGRAM knob (8 variations for each Single effect and 16 variations for each Dual effect). When PROGRAM is set to **User**, selects one of 16 memory locations for user programs.

## Setting Audio Levels

1. Start with INPUT set to 9:00 o'clock and OUTPUT all the way down (fully counter-clockwise).
2. Set the instrument output or effects send being input to the MPX 100 to a nominal level and play, or send audio to the MPX 100. The Level LEDs* should light green.

   If the Clip LEDs light red at this point, turn down the output of the instrument or effects send until the Clip LEDs remain off during the loudest passages.
3. While still sending audio to the MPX 100, gradually turn up the INPUT control until the Clip LEDs show red on only the loudest peaks.
4. Set the MIX control to **Dry**.
5. Turn OUTPUT to the desired level.

* The Level LEDs are off when the incoming signal is low (more than 30dB below overload). The Clip LEDs light red when the signal approaches overload (-2.5dB). Acceptable signals will cause the Level LEDs to light green almost continuously, with the Clip LEDs flashing red on peaks.

**As with any audio product, it is good practice to first power on all outboard gear, then the mixer, then any loudspeakers.**

# The Rear Panel

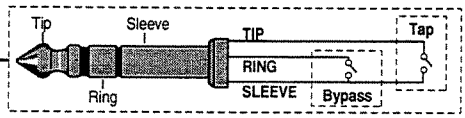
**MIDI**
Two 5-pin DIN MIDI connectors are provided for MIDI IN and software selectable MIDI OUT/THRU.

**POWER**
Use Lexicon 9VAC power pack.

**DIGITAL OUTPUT**
RCA S/PDIF connector.

**OUPUT**
Single-ended (unbalanced) stereo outputs provide +8dBu typical output level. Use the right output connector for mono output. If no connection is made at the right output, the left output can be used to drive headphones at modest volume.


**FOOTSWITCH**
1/4" TRS connector, for momentary contact footswitch, allows footswitch control of front panel Tap and Bypass functions.




**INPUT**
Single-ended (unbalanced) inputs accept levels as low as -30dBu. Input impedance is 500 kΩ. Use the right input for mono sources. Can be used as direct input for guitar.

## Audio Connections

Audio connections to the MPX 100 are unbalanced and should be made with high quality shielded cables with 1/4" tip-sleeve phone plugs at the MPX 100 end.

The MPX 100 produces effects from either mono or stereo sources. With mono sources, the dry signal appears, along with audio effects, at both outputs. For instruments and sources with stereo outputs, use both inputs. We recommend using the outputs in stereo whenever stereo inputs are used, but if mono output is required, use the right output jack. The left and right signals are summed internally when only the right output is used.

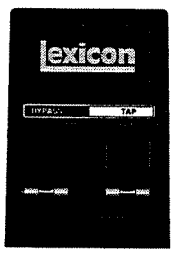
## Headphones

A stereo signal which is adequate to drive headphones is available at the left output (provided no connections are made through the right output). This feature is provided as a convenience for practice purposes, and is intended to provide only modest volume.

## Footswitch

A footswitch connected via the rear-panel footswitch jack allows control of Tap and Bypass. A momentary footswitch can be wired to a tip-ring-sleeve connector. A stereo Y-connector allows two identical single switches to be used.

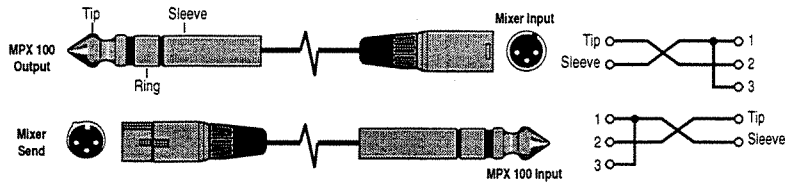
Power off the MPX 100 before plugging in the footswitch. (Otherwise, Bypass will be enabled.)



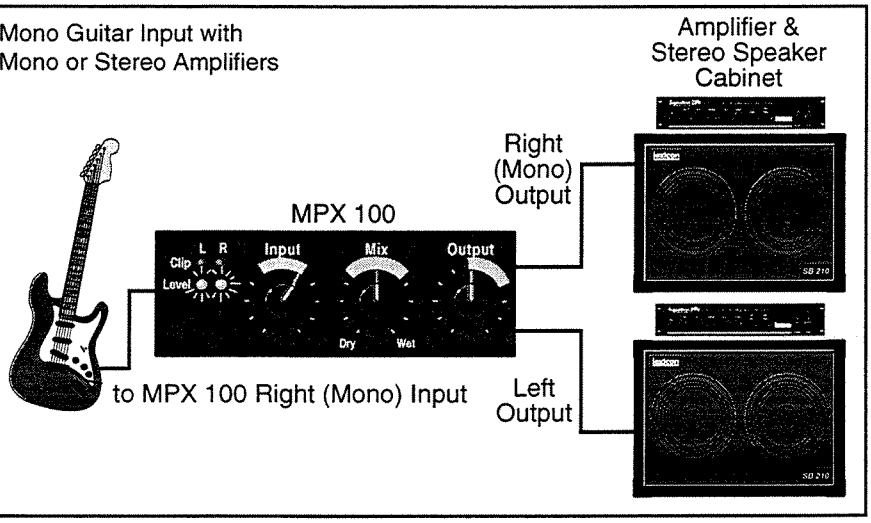

*A dual-function footswitch with a set of labels to identify footswitch functionality (Tap and Bypass) is available from Lexicon dealers.*

The MPX 100 can be used as two independent Effects Processors with Dual Program Variations 11-16. Designate two auxiliary sends on your console and connect one to the left MPX 100 input, and the other to the right input. Refer to the Program Descriptions in the MPX 100 User Guide for programs that use this configuration.

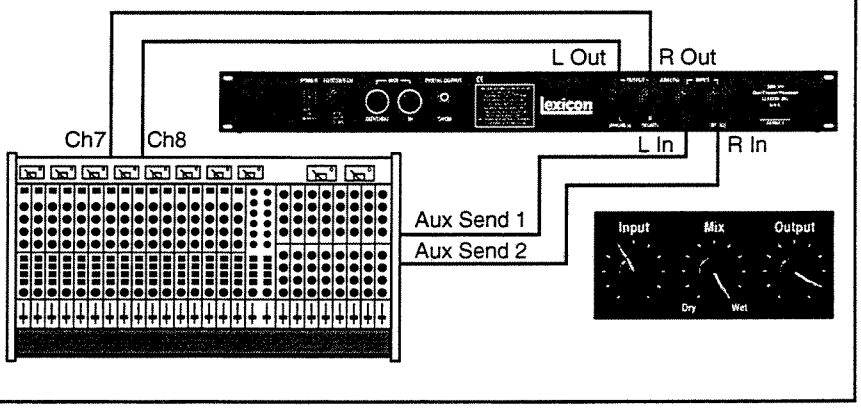
Connecting to a Balanced Console




Mono Guitar Input with Mono or Stereo Amplifiers




Dual Processor Setup with a Console



## Periodic Maintenance

Under normal conditions the MPX 100 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

**Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners.**

Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

## Ordering Parts

When ordering parts, identify each part by type, value and Lexicon Part Number. Replacement parts can be ordered from:

Lexicon, Inc.
3 Oak Park
Bedford MA 01730-1441
Telephone:781-280-0300
Fax: 781-280-0499

ATT: Customer Service

## Returning units for service

**Before returning a unit, for warranty or non-warranty service, consult with Lexicon to determine the extent of the problem, and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.**

If you choose to return an MPX 100 to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured, and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Street address
- City, State, Zip Code, Country
- Telephone number (including Area Code)
- Serial number of unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, both inside and outside of package

Please enclose a brief note describing conversations with Lexicon personnel and give the name and telephone number of the person directly responsible for maintaining the unit.

**Do not include accessories such as manuals, cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Service personnel.**

# 2 Specifications

**Audio Inputs (2)**
*Level* -30dBu to +4dBu
*Impedance* 500K unbalanced for Direct Instrument input
(Unit detects a mono input on the right input)
1/4" connectors

**Audio Outputs (2)**
*Level* +8dBu typical
*Impedance* 75Ω for Headphone output
(Right only used for mono output; Left only used for stereo headphones)
1/4" connectors

**Digital Audio Output**
20-bit Digital S/PDIF output (always active)
*Sample Rate:* 44.1kHz
*Connector:* Coaxial, RCA type

**Footswitch**
Tip/Ring/Sleeve phone jack for Bypass and Tap (optional)

**Frequency Response**
*Dry:* 20Hz-20kHz, ±1dB

**THD+N**
<0.05%, 20Hz-20kHz

**Dynamic Range**
A/A: >95dB typical, 20Hz-20kHz, unweighted
A/D: >100dB typical, 20Hz-20kHz, unweighted

**Conversion**
20 bits A/D, 20 bits D/A
44.1kHz sample rate

**Crosstalk**
>45dB

**Internal Audio Data Path**
*DSP:* 24-bit

**Power Requirements**
9VAC wall transformer provided, 1.9amps

**Dimensions**
19"W x 1.75"H x 4"D (483 x 45 x 102mm)

**Weight**
Unit: 2 lbs, 2 oz (0.959kg)

**Environment**
*Operating Temperature* 32° to 104°F (0° to 40°C)
*Relative Humidity* 95% non-condensing

***Specifications subject to change without notice.***

# 3 Performance Verification

## Required Equipment

- Clean, antistatic, well lit work area
- Digital Volt Meter
- Low Distortion Sine Wave Audio Oscillator
- Distortion Analyzer and Level Meter with single-ended or balanced input, switchable 30kHz high-pass filer or audio bandpass (20-20kHz) filter
- Stereo Headphone Amplifier
- 2 Audio cables unbalanced and shielded with phone plugs on one end and appropriate connectors on the opposite ends for headphone amplifier input
- 2 Audio cables unbalanced and shielded with phone plugs on one end and appropriate connectors on the opposite ends for the Audio Oscillator output
- 9V AC adapter (Lexicon type or equivalent; 1 amp min., 1.9 amp preferred)
- Double Footswitch, Lexicon, or Marshall Model #FS02 or equivalent
- Cable (6ft minimum) with 1/4" to 1/4 stereo phone plugs (Switchcraft# 10BK10 or equivalent)

## Initial Inspection

Inspect the unit for any obvious signs of physical damage. Verify that the front panel controls operate smoothly and correctly. ( Refer to the MPX 100 Owner's Manual for detailed explanations of functionality.) Verify that all screws and rear panel jacks are secure, and inspect the AC power supply for any signs of physical damage.

## Power Up

1. Connect the 9VAC adapter (provided with the MPX 100) between the isolated variable output of the Variac and the MPX 100 rear panel **Power** connector.
2. Verify that AC current draw is <0.1 Amps

On normal power up the MPX 100 will run the following Diagnostic Tests. This Diagnostic Test sequence is displayed on the front panel LEDs for trouble-shooting purposes. If any of the red **Clip** LEDs remain lit, a diagnostic failure has occurred and the MPX 100 should be repaired before proceeding.

| Test No. | Test | Edit | Bypass | Store | Tap |
|---|---|---|---|---|---|
| 1 | ROM Checksum | ● | ● | ● | ○ |
| 2 | SRAM | ● | ● | ○ | ● |
| 3 | Lexichip 3 WCS | ● | ● | ○ | ○ |
| 4 | Lexichip 3 Interrupt Timer | ● | ○ | ● | ● |
| 5 | Lexichip 3 Audio Data File | ● | ○ | ● | ○ |
| 8 | EEPROM Checksum | ○ | ● | ● | ● |

● =OFF
○ =ON

## Functional Tests

### Setup

1. Connect a 5-pin MIDI cable between the MPX 100 rear panel MIDI IN and OUT/THRU connectors.
2. Connect a dual style 1/4" Footswitch to the MPX 100 rear panel Footswitch jack.
3. Turn the MPX 100 front panel VARIATION knob to **12**.
4. Press and hold the MPX 100 front panel **Bypass** button while powering on the MPX 100.
5. When the green **Level** LEDs light, release **Bypass**.
6. Verify that the MPX 100 front panel **Edit** and **Bypass** LEDs are lit.


## Encoder/Switch/LED Test

1. Turn VARIATION to **6** and verify that the **Bypass**, and **Store** LEDs are lit.


2. Press **Store** to initiate the Encoder Test.

### Encoder Test

1. Verify that the green **Level L** LED is lit.
2. Turn the VARIATION encoder clockwise direction one position at a time, and verify that the green **Level L** LED turns off after the encoder has been turned one complete revolution. This indicates successful completion of the VARIATION encoder test. The **Level R** LED should now light.
3. Turn the PROGRAM encoder clockwise one position at a time, and verify that the **Level R** LED turns off after the encoder has been turned one complete revolution. This indicates successful completion of the PROGRAM encoder test.
4. Verify that all of the front panel LEDs are now off.

### Switch/LED Test

1. Press and hold down the Right button on the footswitch. Verify that the green **Level R** LED is on. Release the footswitch and verify that the LED turns off.
2. Press and hold down the Left button on the footswitch. Verify that the green **Level L** LED is on. Release the footswitch and verify that the LED turns off.
3. Press and hold the front panel **Bypass** button. Verify that its LED is on. Release **Bypass** and verify that the LED turns off.
4. Press and hold the front panel **Tap** button. Verify that its LED is on. Release **Tap** and verify that the LED turns off.
5. Press and hold the front panel **Store** button. Verify that its LED is on. Release **Store** and verify that the LED turns off. Releasing **Store** also exits the test series and should cause both of the green **Level** LEDs to turn on.

## ADC Pot Test

Note: During the ADC Pot Test, each potentiometer must be varied over its entire range from fully counter-clockwise to fully clockwise, and back to fully counter-clockwise within 5 seconds. Otherwise the test will fail due to a time-out error. Be prepared, therefore, to move the **Mix** pot as soon as the test is initiated.

1. In preparation for the test, turn the **Mix**, **Effects Lvl/Bal** and **Adjust** pots fully counter-clockwise.
2. Turn VARIATION to **7** and verify that the **Bypass**, **Store** and **Tap** LEDs are on, as shown below.


3. Press **Store** to initiate the ADC Pot Test. The **Level L** LED will light to indicate the test has begun and the **Mix** pot is under test.
4. Move **Mix** from its fully counterclockwise position to fully clockwise, and back within 5 seconds. The **Level L** LED will flash to indicate the **Mix** pot has passed and the **Level R** LED will light.
5. Move **Effect Lvl/Bal** from its fully counterclockwise position to fully clockwise, and back within 5 seconds. The **Level R** LED will flash to indicate the **Effect Lvl/Bal** pot has passed, then both **Level** LEDs will light.
6. Move **Adjust** from its fully counterclockwise position to fully clockwise, and back within 5 seconds. Both **Level** LEDs will flash to indicate the **Adjust** pot has passed, then the **Level** LEDs will light steadily to indicate the ADC Pot Test is complete.

## Midi Wraparound Test

1. Turn VARIATION to the **9** and verify that the **Edit** and **Tap** LEDs are lit as shown below.


2. Press **Store** to execute the test.
3. The **Level** LEDs will light to indicate the test has been successfully completed.

## Listening Test

This test involves running audio through the MPX 100 with and without effects processing. This is helpful in differentiating audio problems in the analog from the digital circuitry. The first part of this test is performed without effects.

**Setup**

1. Connect two audio cables between connect the MPX 100 rear panel Left and Right Outputs and the headphone amplifier Left and Right Inputs.
2. Attach the single end of a Y-connector into the output of the sine wave audio oscillator, and the Y end into the MPX 100 Left and Right Inputs.
3. Set the headphone amplifier volume control to its lowest level.
4. Press and hold down the front panel **Bypass** button while powering on the MPX 100. Continue to hold **Bypass** until the Power On Diagnostics are completed and the green **Level** LEDs light.
5. Turn VARIATION to **13**, and verify that the **Edit**, **Bypass** and **Tap** LEDs are on, as shown below.


6. Press **Store** to execute the test.
7. Input a 1kHz sine wave at 0dBu to the MPX 100.
8. Turn the MPX 100 **Input**, **Mix**, **Output**, **Effect Lvl/Bal**, and **Adjust** knobs fully clockwise.
9. Put on headphones, then set the headphone amplifier volume to a comfortable listening level.
10. Individually adjust the MPX 100 **Input** and **Output** knobs over their entire range and verify that no pops, clicks, or scratchiness is heard.

## Effects Listening Test

1. Turn VARIATION to **14** and press Store to return to normal operating mode.
2. Verify that the processed audio has no audible pops, clicks, or distortion.

## Shock Test

1. Lift each corner of the MPX 100 off the bench 4 inches (4") then drop. **To prevent damaging the unit, keep one corner of the unit touching the bench at all times.**
2. Verify that no audio, or LED intermittence is caused by this action.

## Audio Performance

### Oscillator and Analyzer Default Settings

Unless otherwise noted the following settings are used for the audio performance tests:

| Oscillator | | Analyzer | |
|---|---|---|---|
| Waveform: | Sine | Filter: | Off |
| Output: | Unbal | Bandwidth: | 22Hz to 22kHz |
| | –25Ω | Inputs: | 100kΩ |
| | Float | | (except Gain=600Ω) |

### Setup

1. Connect the appropriate cable between the oscillator output and the MXP 100 Left input.
2. Connect the appropriate cable between the analyzer input and the MPX 100 Left output.
3. Turn the MPX 100 front panel **Input** and **Output** knobs fully clockwise.
4. Turn the MPX 100 front panel **Mix** knob fully counterclockwise.
5. Power cycle the MPX 100 while pressing and holding down the **Bypass** button. Wait until the **Level** LEDs light, then release **Bypass**.
6. Turn VARIATION to **13** and press **Store** to set up the MPX 100 for the following tests.

## Gain Test

This test verifies the input-to-output gain characteristic of the MPX 100 through the signal path.

1. Apply a 1kHz signal at 775mV to the MPX 100
2. Verify 1.95 V +/- 0.05V at the MPX 100 Left output.
3. Connect the oscillator output to the MPX 100 Right input.
4. Connect the analyzer input to the MPX 100 Right output.
5. Verify an output of 1.95V +/- 0.05V at the MPX 100 Right output.

## Signal-to-Noise

This test checks the signal-to-noise through the MPX 100 signal path.

1. Set the scale on the distortion analyzer to measure -50dBu signal.
2. Disconnect the oscillator from the MPX 100 input, or turn the oscillator off.
3. Verify that the noise floor is <90dBr.
4. Connect the oscillator output to the MPX 100 Left input.
5. Connect the analyzer input to the MPX 100 Left output.
6. Repeat the test, verifying the levels at the Left output.

This test verifies THD+N through the MPX 100 signal path.

## THD+N

1. Apply a 1kHz signal at 220mV to the MPX 100 left input.
2. Adjust the scale on the distortion analyzer to measure % THD+N.
3. Verify a distortion level <0.05% THD+N at the Left output.
4. Connect the oscillator output to the MPX 100 right input.
5. Connect the analyzer input to the MPX 100 right output.
6. Verify a distortion level <0.05% THD+N at the right output.

## Frequency Response

This test verifies the frequency response of the MPX 100 through the signal path at 20Hz, 3kHz, 5kHz, and 20kHz.

1. Apply a 220mV signal at 1kHz with the analyzer Bandwidth filters off to the MPX 100 Right input.
2. Use the output level at the MPX 100 Right output for the 0DB reference to check frequency response.
3. Verify that the signal level output is within ±0.5dB of the reference at the above frequencies.
4. Connect the oscillator output to the MPX 100 Left input.
5. Connect the analyzer input to the MPX 100 Left output.
6. Repeat the test, verifying levels for the MPX 100 Left output.

## Power Supply

1. Remove cover as described in disassembly/reassembly section.
2. Plug the adapter into the MPX 100 and apply power.
3. Set the DMM to measure VD and check the regulated voltages for proper levels.

| Supplies | Location | Range |
|---|---|---|
| +5 VD | Marked test points to the Right of C6 | (4.85-5.25) |
| +5 VA | Marked test points to the Left of J6 | (4.75-5.25) |
| -5 VA | Marked test points to the Left of J6 | (4.75-5.25) |

## Restoring Factory Settings

**Caution, this Procedure will destroy any user settings or registers.**

1. Power up the MPX 100, then press and hold the **Bypass**.
2. Turn VARIATION to **15**.
3. Press **Store**.
4. The MPX 100 will clear the registers then cycle through a normal power up and return to normal running mode

## Disassembly/Reassembly

### Disassemby

1. Remove six (6) screws from the housing: three (3) from the top, and three (3) from the bottom.
2. Carefully remove the two end caps, swinging them out by the rack ears.
3. Remove five (5) plastic nuts from the jacks on the rear panel.
4. Remove the two (2) small Phillips head screws at the rear panel MIDI jacks.
5. Holding the front panel, carefully remove the cover.
6. To disconnect the circuit board from the front panel:
   a. Pull off the seven (7) knobs on the front panel
   b. Remove the seven (7) nuts and washers from the front panel.
   c. Hold the unit face down, and carefully separate the circuit board assembly from the front panel.
   d. Carefully remove the buttons from the rear of the front panel.
   NOTE: The buttons are loose and can fall out.

### Reassembly

1. Holding the front panel face down, reinsert the buttons. Continue to hold the front panel face down so as not to loosen the buttons.
2. From the rear, carefully position the circuit board and insert it into the front panel.
3. Replace the nut and washer on one potentiometer at each end and hand tighten.
4. Replace the remaining potentiometer nuts and washers. Check for alignment, then tighten all nuts. Do not overtighten.
5. Replace the cover, being careful to align the jacks and power connector with the holes in the rear of the cover.
6. Replace the seven (7) plastic nuts on the jacks. Be careful not to overtighten.
7. Replace the seven (7) knobs on the front panel.
8. Replace the two (2) screws at the rear panel MIDI jacks.
9. Insert the two end caps by hooking the rear tab of each into each end of the cover.
10. Holding the end caps in place, install the six (6) screws.
11. Tighten the rear-panel screws next to the power connector.

## Removal and Installation of Components

From time to time, it may be necessary to replace pots, jacks or other components. When desoldering, be careful not to overheat the board. Use all caution to prevent damage to the circuit board, traces and pads.

When installing pots, jacks or displays, make sure that they are mechanically flush with the circuit board prior to soldering in place. If not properly aligned, stress can be placed on the new components and the board, resulting in early failure of the board and/or component.

# Diagnostics/ Troubleshooting

## Diagnostics

There are two diagnostic sets in the MPX 100: Power On Diagnostics which are run when the unit is powered up, and Extended Diagnostics which are designed to facilitiate troubleshooting.

### Power On Diagnostics

The Power On Diagnostics first cause all of the MPX 100 front panel LEDs to light (for approximately 200ms), then executes a series of tests, lighting a test code on the front panel to identify which test is being run. The entire Power On procedure takes approximately 10 seconds.

The following table shows the sequence of tests and each identifying LED code

| Test No. | Test | Edit | Bypass | Store | Tap |
|---|---|---|---|---|---|
| 1 | ROM Checksum | ● | ● | ● | ○ |
| 2 | SRAM | ● | ● | ○ | ● |
| 3 | Lexichip 3 WCS | ● | ● | ○ | ○ |
| 4 | Lexichip 3 Interrupt Timer | ● | ○ | ● | ● |
| 5 | Lexichip 3 Audio Data File | ● | ○ | ● | ○ |
| 8 | EEPROM Checksum | ○ | ● | ● | ● |

● =OFF
○ =ON

If the Power On Diagnostics tests are completed successfully, the display will briefly flash the software version in the MPX 100.

### Diagnostic Failures

If a test fails, testing will be halted, the audio outputs will be muted, and both red **Clip** LEDs will light along with the LED code for the failed test.

When this occurs, you have three options:

1. Press **Bypass** to proceed to the next test. This may help determine multiple test failures. **CAUTION**

   **Bypassing a failed test may result in excessive speaker excursion and/or loss of user register data.**
2. Press **Store** to enter Extended Diagnostics Mode which allows more thorough testing of the unit.
3. Press **Tap** to have the MPX 100 continuously run the failed test while you examine the circuitry.

## Power Up Diagnostics Test Descriptions

Before each test is executed, its test code will be displayed on the front panel LEDs. These codes are ncluded in the following descriptions.

● =OFF
○ =ON

### 1 ROM Checksum

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ● | ● | ○ |

This test verifies the ROM checksum by sending it a byte-size value that is stored in the last location of Bank 0. The test then adds the contents of the entire ROM including the Checksum byte. The result should equal zero (8 bit value).

If a failure occurs, the CPU will automatically attempt to continuously loop the test for troubleshooting purposes.

### 2 SRAM

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ● | ○ | ● |

The SRAM Test destructive. The entire contents of the SRAM is tested by first writing 00 hex (00000000 binary) to all of the memory locations, and reading back all of the memory locations. The test is repeated by writing/reading the following patterns: 55 hex (01010101 binary), AA hex (10101010 binary) & FF hex (11111111 binary).

If a failure occurs, the CPU will automatically attempt to continuously loop the test for troubleshooting purposes.

### 3 Lexichip 3 WCS

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ● | ○ | ○ |

This test checks the program memory space (WCS) of the Lexichip 3. RAM memory space is first filled with the value 55 hex (01010101 binary), then each memory location is read to see if it contains 55. This test is repeated with AA hex (10101010 binary), and then 0"s. Following this test an Address test is implemented to verify all the address lines are active. Finally, the memory is checked for 0's.

### 4 Lexichip 3 Interrupt Timer

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ○ | ● | ● |

The Interrupt Timer test verifies the functionality of the interrupt (INT/) signal. The Lexichip 3 provides the interrupt (INT/) to the Z80's maskable interrupt line. The test allows 20 interrupts to be sent by Lexichip 3 to the Z80's maskable interrupt line. A count of the interrupts is kept and compared for overshoot and undershoot. More han 21 interrupts means the interrupt is too short; less than 19 interrupts means it is too long.

### 5 Lexichip 3 Audio Data File

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ○ | ● | ○ |

The Audio Data File (ADF) is a fast synchronous 128-word SRAM that provides audio data buffering and storage for: external memory references, Serial I/O, and the Host-to-Lexichip data port. ADF locations also function as ARU Registers and as scratch pad memory. This test verifies that the Lexichip 3 Audio Data File is working properly.

## Extended Diagnostics

To enter the MPX 100 Extended Diagnostics mode, press and hold **Bypass** while powering on the MPX 100. When the green **Level** LEDs light, release **Bypass**. The green **Level** LEDs will go off and the **Edit**, **Bypass**, **Store** and **Tap** LEDs will display the test code corresponding to the current position of the VARIATION knob in binary.

● =OFF
○ =ON

For example, if VARIATION were set to **5**, the LEDs would read:

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ○ | ● | ○ |

Pressing **Store** will execute the selected test. If the test passes, both green **Level** LEDs will light. If the test fails, the both red **Clip** LEDs will light. Pressing **Tap** instead of **Store** will run certain tests continuously.

The following table shows the Extended Diagnostics tests which can be selected with VARIATION along with their binary codes. Note that tests 1-5 are identical to the Power On Diagnostics tests of the same name. Those tests which can be set into looping behavior with **Tap** are noted.

| VARIATION Setting | Test Name | Binary Code | Loops when activated by Tap |
|---|---|---|---|
| 1 | ROM Checksum | 0 0 0 1 | X |
| 2 | SRAM Test | 0 0 1 0 | X |
| 3 | Lexichip 3 WCS | 0 0 1 1 | X |
| 4 | Lexichip 3 Interrupt Timer | 0 1 0 0 | X |
| 5 | Lexichip 3 Audio Data File | 0 1 0 1 | X |
| 6 | Encoder/Switch/LED* | 0 1 1 0 | - |
| 7 | ADC Pot** | 0 1 1 1 | - |
| 8 | EEPROM | 1 0 0 0 | X |
| 9 | MIDI | 1 0 0 1 | X |
| 10 | LED (for troubleshooting)* | 1 0 1 0 | - |
| 11 | Lexichip 3 External DRAM | 1 0 1 1 | X |
| 12 | Burn In Loop | 1 1 0 0 | - |
| 13 | Audio I/O | 1 1 0 1 | - |
| 14 | Exit Diagnostics | 1 1 1 0 | - |
| 15 | Initialize | 1 1 1 1 | - |

* Requires operator interaction and judgment. Does not generate any error messages.
** Requires operator interaction and judgment. Generates an error message.

When a test is run continuously, its pass/fail status will be displayed and updated on the headroom LEDs each time the test is run. To stop a looping test, press **Store.**

### 1 ROM Checksum

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ● | ● | ○ |

This test verifies the ROM checksum by sending it a byte-size value that is stored in the last location of Bank 0. The test then adds the contents of the entire ROM including the Checksum byte. The result should equal zero (8 bit value).

If a failure occurs, the CPU will automatically attempt to continuously loop the test for troubleshooting purposes.

### 2 SRAM

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ● | ○ | ● |

The SRAM Test destructive. The entire contents of the SRAM is tested by first writing 00 hex (00000000 binary) to all of the memory locations, and reading back all of the memory locations. The test is repeated by writing/reading the following patterns: 55 hex (01010101 binary), AA hex (10101010 binary) & FF hex (11111111 binary).

If a failure occurs, the CPU will automatically attempt to continuously loop the test for troubleshooting purposes.

### 3 Lexichip 3 WCS

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ● | ○ | ○ |

This test checks the program memory space (WCS) of the Lexichip 3. RAM memory space is first filled with the value 55 hex (01010101 binary), then each memory location is read to see if it contains 55. This test is repeated with AA hex (10101010 binary), and then 0"s. Following this test an Address test is implemented to verify all the address lines are active. Finally, the memory is checked for 0's.

### 4 Lexichip 3 Interrupt Timer

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ○ | ● | ● |

The Interrupt Timer test verifies the functionality of the interrupt (INT/) signal. The Lexichip 3 provides the interrupt (INT/) to the Z80's maskable interrupt line. The test allows 20 interrupts to be sent by Lexichip 3 to the Z80's maskable interrupt line. A count of the interrupts is kept and compared for overshoot and undershoot. More han 21 interrupts means the interrupt is too short; less than 19 interrupts means it is too long.

### 5 Lexichip 3 Audio Data File

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ● | ○ | ● | ○ |

The Audio Data File (ADF) is a fast synchronous 128-word SRAM that provides audio data buffering and storage for: external memory references, Serial I/O, and the Host-to-Lexichip data port. ADF locations also function as ARU Registers and as scratch pad memory. This test verifies that the Lexichip 3 Audio Data File is working properly.

**6 Encoder/Switch/LED** **Edit** ● **Bypass** ○ **Store** ○ **Tap** ●

When this test is executed, the green **Level L** LED will be lit, and all Front Panel LED's will be turned off.

**NOTE: The Encoder/Switch/LED Test must be performed in the proper sequence — with the Encoder portion of the test first.**

Encoder Test
NOTE: The encoder must be rotated *clockwise* or the test will fail. During the test, the front panel LEDs will display the current position of the encoder under test. (See table below.)

| PROGRAM | VARIATION | Binary Code |
|---|---|---|
| Plate, Gate | 1 | 0 0 0 1 |
| Hall, Chamber | 2 | 0 0 1 0 |
| Ambience, Room | 3 | 0 0 1 1 |
| Tremelo, Rotary | 4 | 0 1 0 0 |
| Chorus, Flange | 5 | 0 1 0 1 |
| Pitch, Detune | 6 | 0 1 1 0 |
| Delay, Echo | 7 | 0 1 1 1 |
| Special FX | 8 | 1 0 0 0 |
| User | 9 | 1 0 0 1 |
| Flange - Delay | 10 | 1 0 1 0 |
| Pitch - Delay | 11 | 1 0 1 1 |
| Chorus - Delay | 12 | 1 1 0 0 |
| Delay - Reverb | 13 | 1 1 0 1 |
| Flange - Reverb | 14 | 1 1 1 0 |
| Pitch - Reverb | 15 | 1 1 1 1 |
| Chorus - Reverb | 16 | 0 0 0 0 |

When the Encoder Test is activated, the green **Level L** LED will be lit to indicate that VARIATION is being tested. Turn VARIATION clockwise over its entire range. The **Level L** LED will turn off to indicate the encoder has passed and the **Level R** LED will light to indicate the PROGRAM encoder is being tested.

Turn PROGRAM clockwise over its entire range. The **Level R** LED will turn off to indicate that the encoder has passed, and the Footswitches and Front Panel Switches are ready to be tested.

If the PROGRAM test fails, the red **Clip R** LED will light.

**Footswitches**
This test requires a dual-function footswitch (as described on page 5 of the MPX 100 User Guide).

When the left footswitch (Ring) is pressed, the green **Level L** LED will light. The other front panel LEDs will be off. When the left footswitch is released, the **Level L** LED will turn off.

When the right footswitch (Tip) is pressed, the green **Level R** LED will light. The other front panel LEDs will be off. When the left footswitch is released, the **Level R** LED will turn off.

To test the front panel switches, proceed to the next section. To exit testing, press and hold **Store** for a few seconds, then release. The front panel LEDs will display the binary code for the current position of the VARIATION encoder.

### Front Panel Switches

Press each of the front panel switches in turn: **Bypass**, **Tap** and **Store.** When any of these switches is depressed, its LED will light and remain lit as long as the button is depressed. When the button is released, its LED will turn off.

### Encoder Gray Scale

The following table is provided as a reference for debugging encoder problems.

| Encoder Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| Pin 2 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| Pin 3 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| Pin 4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Pin 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**NOTE: The logic levels from the encoders are only valid when the enable (pin 5) is low.**

### 7 ADC Pot Test

**Edit** ● **Bypass** ○ **Store** ○ **Tap** ○

The **Mix**, **Effects Lvl/Bal** and ADJUST pots are connected to integrating A/D Converters (ADCs) which are read digitally by the Lexichip 3. This test verifies that each pot and the converters are functioning properly. During each test, the pot must be turned over its entire range from fully counterclockwise to fully clockwise and back to fully counterclockwise (CCW–>CW–>CCW).

NOTE: The ADC Pot Test must be performed in the proper sequence — starting with the **Mix** pot. As each pot must be turned within 5 seconds of test activation, turn all three pots fully counterclockwise and be prepared to Move **Mix** immediately after initating the test series with the **Store** button.

When the ADC PotTest is activated, the green **Level L** LED will be lit to indicate that the **Mix** test is armed. Turn **Mix** CCW–>CW–>CCW. The **Level L** LED will flash briefly to indicate **Mix** has passed, then the **Level L** LED will turn off and the **Level R** LED will turn on to indicate the **Effects Lvl/Bal** test is armed.

Turn **Effects Lvl/Bal** CCW–>CW–>CCW. The **Level R** LED will flash briefly to indicate that the pot has passed, then both **Level** LEDs will light to indicate the ADJUST pot is ready to be tested.

Turn ADJUST CCW–>CW–>CCW. Both **Level** LEDs will flash briefly to indicate ADJUST has passed, then both LEDs will light steadily.

**8 EEPROM Checksum** **Edit** ○ **Bypass** ● **Store** ● **Tap** ●

This test reads each byte in the User Register portion of the EEPROM and calculates a checksum. This value is compared with the checksum value stored in the EEPROM itself. This checksum is recalculated each time a register is stored.

Both the green **Level** LEDs will light to indicate the test has passed.

**9 MIDI Tests**

**MIDI Out To MIDI In** **Edit** ○ **Bypass** ● **Store** ● **Tap** ○

This test verifies functionality of the MIDI IN and OUT/THRU circuits. The test transmits data from the MIDI OUT jack and attempts to read the data back through the MIDI IN jack. To run this test, a 5-pin DIN MIDI cable must be connected between the MIDI IN jack and the MIDI OUT jack. MIDI signals are generated by Lexichip 3.

Both the green **Level** LEDs will light to indicate the test has passed.

**MIDI THRU To MIDI IN**

MPX 100 MIDI THRU circuitry is verified with Lexicon ATE test procedures. The test programs and utilities are available, unsupported, for service centers using the Audio Precision brand test equipment set. Contact Lexicon Customer Service.

**10 LED Test** **Edit** ○ **Bypass** ● **Store** ○ **Tap** ●

This test verifies the functionality of all front panel LEDs. When the test is activated, the front panel LEDs (**Clip L**, **CLip R**, **Level L**, **Level R**, **Edit**, **Bypass**, **Store** and **Tap)** should light in response to repositioning of the PROGRAM knob as shown below.

| **PROGRAM Postion** | **LED Status** |
|---|---|
| Plate, Gate | All On |
| Hall, Chamber | Clip L On |
| Ambience, Room | Clip R On |
| Tremelo, Rotary | Level L On |
| Chorus, Flange | Level R On |
| Pitch, Detune | Edit On |
| Delay, Echo | Bypass On |
| Special FX | Store On |
| User | Tap On |
| Flange - Delay | All Off |
| Pitch - Delay | All Off |
| Chorus - Delay | All Off |
| Delay - Reverb | All Off |
| Flange - Reverb | All Off |
| Pitch - Reverb | All Off |
| Reverb | All Off |

### 11 Lexichip 3 External DRAM Test

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ○ | ● | ○ | ○ |

This test puts the Lexichip 3 (U5) into a mode that allows the Z80 processor (U7) to read and write to the 1M X 4 DRAM (U3) through the Lexichip 3. To actually test the DRAM, the Z80 processor performs two tests: a data test and an address test. During the data test the Z80 processor writes "AA" (hex) (10101010) into all of the memory locations then reads them back. It repeats the process with "55" (01010101). For the address test, the Z80 processor writes a count into the memory then reads it back (i.e.00000001, 00000010, 00000011).

### 12 Burn-In Loop

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ○ | ○ | ● | ● |

The Burn In Loop runs the following tests continuously.

| Test Name | Binary ID Code |
|---|---|
| 1 | ROM Checksum0 0 0 1 |
| 2 | SRAM Test 0 0 1 0 |
| 3 | Lexichip 3 WCS0 0 1 1 |
| 4 | Lexichip 3 Interrupt Timer 0 1 0 0 |
| 5 | Lexichip 3 Audio Data File 0 1 0 1 |
| 11 | Lexichip 3 External DRAM 1 0 1 1 |

During the execution of the Diagnostics in the Burn-In Loop, the binary code for each test will be displayed before the test is executed. If a test fails, the red **Clip** LEDS will light, the Burn-In Loop will stop and the LEDs will display the binary code for the failed test.

There are three options available when a test has failed during the Burn In Loop:

1. Press **Bypass** to continue the Burn In Loop.
2. Press **Tap** to run the failed test continuously.
3. Press **Store** to exit the Burn-In Loop.

### 13 Audio I/O

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ○ | ○ | ● | ○ |

The Audio I/O Test sets the audio path through the MPX 100 to 100% wet with all effects turned off. This allows you to eliminate major functional sections of the system when troubleshooting distortion noise, gain, crosswalk and frequency response problems.

### 14 Exit Diagnostics

| Edit | Bypass | Store | Tap |
|---|---|---|---|
| ○ | ○ | ○ | ● |

This selection allows you to exit Extended Diagnostics and return to normal operating mode.

**15 Initialize** **Edit** **Bypass** **Store** **Tap**

This selection resets all MPX 100 parameters to their factory defaults.

NOTE: Performing this test will clear any registers stored in the MPX 100. To save them, download them before initializing, then reload them when the test is done.

# 4 Theory of Operation

## Schematic Walkthrough

### Sheet 1

This sheet shows the analog input section (U20-22), ADC (U17), DAC (U13), analog output section (U16, 18- 19) and their associated circuitry, as well as the output mute circuit (U18).

### Input Stage

Separate unbalanced 1/4" unbalanced phone jacks (J8 and J9) are provided for left and right input signals. A single input source will be routed to both left and right input stages if only the right input (J9) is used. J8 and J9 also provide chassis ground through an integrated ground lug from the PCB to the cover.

Capacitors (C75 and C86) are found at the inputs to prevent unwanted high frequency interference from entering or leaving the MPX 100 through the input cables.

DC blocking is incorporated by capacitors (C74 and C85) in line with the signal path.

The input impedance of the MPX 100 is set by R110 and R124, 1MΩ per channel and 500KΩ when summed to mono by plugging in the Right I/P only. This allows the MPX 100 to be used with a wide variety of input sources, including electric guitars. Because of the high input impedance, the input is very susceptible to noise pickup from radiating sources. This is not a problem with an instrument plugged in as the instruments relatively low (1k-10k) output impedance provides a path to ground.

When the plug is empty, however, there is a full 1Meg for a noise voltage to form across. For this reason, the left and right inputs short to ground when empty.

D24 and D25 protect U20 and U22 from large input signals. R111 and R123 limit the current through D24 and D25 during conduction to protect them. This insures signals at the input of the U20 and U22 are never greater than 0.7V above the op-amp rails.

The non-inverting inputs of one-half U20 and U22 are used as the signal input buffer to maintain a high input impedance, to provide unity gain at low frequencies, and to provide pre-emphasis.

R112, R113, C78 and R121, R122, C91 comprise feedback networks around U20 and U22, respectively which form a high pass shelf for pre-emphasis. It is a 10dB shelf starting at 3kHz and ending at 9kHz. This is a 15/50uS curve with matching de-emphasis on the output. Capacitors C79, C92 provide high frequency compensation for this input buffer stage.

C96 and C97 remove offset, so potentiometer wiper noise in R116 is eliminated. R116 is a ganged dual pot for input level control.

The second half of U20 and U22 is a gain stage which provides approximately 25db of gain. R114, R115 and R125, R126 set the gain of the respective channels. C82 and C95 are used for op-amp compensation at high frequencies. C80, C81, and C93, C94 are power supply bypass capacitors for U20 and U22.

U21 provides a unity gain inverting stage. This, in conjunction with the output of the prior gain stage, provides the differential input to the CS5335 A/D converter (U17). R117, R118 and R119, R120 set the gain to unity. C87 and C90 provide high frequency compensation for this inverting stage. C88 and C89 are power supply bypass capacitors for U21.

Capacitors C76, C83 and C77, C84 block the 2.5VDC level shift generated by the self-biasing of the CS5335 A/D (U17) inputs. The combined output of the inverting stage and the non-inverting gain stage provide 6db more gain at the differential inputs of the A/D. This guarantees full scale input to the A/D converter with a low level input signal.

R106, R107, C70 and R109, R108, C71 provide anti-aliasing filters before the conversion. The corner frequency of this filter is 240kHz.

R99, C63, C65 and C62, C64 filter the analog 5V supply for the ADC.

**A/D** The Crystal CS5335 (U17) is a complete stereo analog-to-digital converter which performs anti-alias filtering, sampling and A/D conversion, generating 24-bit values for both left and right inputs in serial form. The CS5335 operates in slave mode where SCLK and LRCLK are inputs.

Data is clocked in on the rising edge of the bit clock (64FS) and is aligned with the second bit clock following the leading edge of each transition in the LRCLK (FS). This alignment is determined by setting the serial data interface format pins on the CS5335 to support the I2S format. The Lexichip 3 Serial Receive port (SDIN0) will need its mode and configuration registers set to accommodate I2S format data.

Upon power-up, the digital filters and delta-sigma modulators are reset, and the internal voltage reference is powered down. The device remains in power down mode until MCLK (256FS, 11.2896MHz) and LRCLK (FS, 44.1kHz) are presented. Once MCLK and LRCLK are detected, MCLK occurrences are counted over one LRCLK period to determine the MCLK/LRCLK frequency ratio. Then, the internal voltage reference is determined, power is applied and the analog inputs will move to approximately 2.2V.

The initialization and settling sequence requires approximately 28672 periods of LRCLK (650mS at a 44.1kHz sample rate). This time is dominated by the settling time required for the integral high pass filter which is enabled to remove DC offset within the A/D converter.

**D/A** The Crystal CS4327 (U13) is a Delta-Sigma architecture digital-to-analog converter. The CS4327 can be configured to operate in a variety of modes. In the MPX 100 the Digital Input Format is set to support the I2S serial protocol.

The DAC is set run from a 256FS MC (the same MC as the A/D). This is generated by the Lexichip 3. Data is clocked in on the rising edge of the bit clock (64FS) and is aligned with the second bit clock following the leading edge of each transition in the LRCLK (FS). This alignment is determined by programming the Lexichip 3 Serial Transmit port (SDOUT0) to support the I2S format.

**Output Stage**

R86, C39, C40, C41 and C42 filter the supplies to the CS4327 DAC (U13).

Coming out of the DAC are capacitors C48 and C49, which remove a 2.2V offset from the DAC. R90 and R94 give U16 inputs a bias current path and references the signal from the DAC to ground.

U16 and its associated components R93, R95 C52, C55 and R89, R91, C50, C54 form a second-order, unity gain, low-pass filter of Sallen-Key type. R96, C58 and R92, C57 form a first-order, low-pass filter. The two filter sets combined form a third-order, anti-imaging filter at 100kHz. C51 and C56 are power supply bypass capacitors for U16.

C53 and C59 are DC blockers which eliminate any offset from U16 to prevent potentiometer wiper noise in R97. R97 is a ganged dual pot for output level control.

Two analog switches (U18) provide output muting during power up and power down conditions. The MUTE/ signal which controls these switches is generated from a control register which is set low on power reset. This signal is terminated at pins 9 and 10 of U18. When MUTE/ is low, pins 4 and 5 of U18 are connected for the right output and pins 15 and 2 of U18 are connected for the left output, creating a low-impedance signal path to ground. These switches are placed in parallel with the output level potentiometer before the output stage. Approximately 43dB of attenuation is achieved when the switch is on. (MUTE/ is low.)

A dual op-amp (U19) and its associated circuitry (R101, R102, C68 and R103, R104, C69) make up the final output stage. This stage provides 10.5dB of gain and the complementary de-emphasis curve to compensate for the pre-emphasis function performed before the conversion process. C67 and C73 are the +V and -V power supply bypass capacitors for U19.

An impedance of 75Ω is developed by R88 and R98 for the left and right outputs, respectively. These resistors also provide current limiting protection. The output 1/4" unbalanced phone jacks (J6 and J7) are configured in such a way that, when only the right jack (J7) is connected, the left and right outputs are summed together to provide a mono output. The left jack (J6) can support stereo headphones if the right jack is not connected. The left channel appears on the tip and the right channel appears on the ring of a stereo phone plug of this three-conductor 1/4" phone jack. C47 and C61 are provided for RFI suppression at the outputs.

Although the output op-amp can drive high-impedance (>100Ω) headphones, it is not designed for low-impedance headphones. For best results, use a headphone amp.

**Sheet 2** This sheet shows the Z80 (U8), ROM (U10), SRAM (U9), Lexichip 3 (U5) and its audio memory (U3), as well as a EEPROM (U2) for non-volatile storage. The pull up/down resistors on the system data bus are used to program the Lexichip 3 operating mode. Upon the rising edge of RESET/, various Lexichip 3 mode bits are set which determine system operating parameters. This is done externally by pull-up/down resistors R59-R66. The 10MHz Z80 (U8) runs at 9.0316MHz.

EPROM location (U10) is 128k (27C010,70ns).

Running the Z80 at 9.0316MHz and using the zero wait states for ROM access accommodates a ROM with an access time of 112nS or better.

8K x 8 SRAM (U9) can have a relatively slow access time, 80ns and faster will operate with one waitstate with the Z80 running at 9.0316MHz.

**Clocks** This chip mode determines various system parameters: Host address decode map, masterclock frequency and source, and Zclock frequency and source. For an audio sample rate of 44.1KHz, the Lexichip 3 crystal input is selected as 11.2896 MHz, the internal PLL bumps this up 4X to a Lexichip 3 master clock frequency of 45.1584 MHz. All other clocks, including ZCLK/ are derived from this Lexichip 3 master clock. The conversion clocks, FS, 64FS, and 256FS are derived from the 11.2896 MHz xtal.

**Audio Memory** The MPX 100 is currently set up to use one 4-bit wide DRAM. This is done by setting the appropriate fields in the Lexichip 3 Sub Mode Control Register 1.

The audio memory complement is a single 60ns, 4Mbit DRAM (1M x 4), U3. Four 4-bit accesses are assembled for a 16-bit word. DRAM address and control lines have the option of using series dampening resistors. These are represented by R18-R30.

**EEPROM** Non-volatile data storage is incorporated with a 2-wire serial/I2C 24C04 (4K bit) EEPROM. This serial EEPROM (U2) uses a two wire bus protocol. U2, pin 5 is the serial address/data input/output. This is a bi-directional pin used to transfer addresses and data into and out of the device. U2, pin 6 is the serial clock input used to synchronize the data transfer to and from the device.

Pins 98 and 96 of Lexichip 3 are configured as PIOB(7) and PIOB(4). PIOB(7)(pin 96) is used to generate the serial clock and PIOB(4)(pin 98) is the bi-directional address/data for the EEPROM.

EEPROM_DATA is pulled high through R17. This signal must remain in a high logic state so that the EEPROM SDA signal can pull this signal to a low logic level to generate an acknowledge pulse after the reception of each byte.

## Sheet 3

Sheet 3 includes the front panel Encoders and Pot A/D.

### Encoders

Pull-up resistors are provided at the front panel encoders (SW3 and SW4). R48-R51 pulls up the inputs to prevent Lexichip 3 inputs from floating and to provide a default non-active switch state of logic high. Diodes D13-D16 (PROGRAM encoder) and D18-D21 (VARIATION encoder) are used to isolate the output of the unselected encoder during the reading of the selected encoder. An encoder is selected when its C pin is set low, allowing the corresponding group of diodes to conduct and indicate the gray-scale code for the selected encoder's current position. A NAND gate (U7) is used as an inverter to ensure exclusive selection of the active encoder.

### Control Input (IAD)

The pot A/D converter is an integrating type, made from current source Q5 and an 8-bit timer in Lexichip 3. To start the conversion, the Z80 tells the Lexichip 3 to bring RESET_IAD high, which toggles U23 and discharges capacitor C38 to less than 0.2V. Next, the Z80 selects which pot (ADMUXIN0 - 3) the Lexichip 3 will digitize by writing to a IAD mux register in the Lexichip 3.

The Lexichip 3 then starts its timer and brings RESET_IAD low. C38 starts to charge from the current source. Once the capacitor voltage exceeds the pot voltage, the muxed comparator output goes low. This disables the Lexichip 3 counter. At its convenience the Z80 reads the timer and derives the voltage on the pot. R80 sets input voltage range from 0-3V. This voltage, which is also the calibration voltage for the IAD, ensures that the pot's full range will be used, regardless of fluctuation in voltage and temperature.

## Sheet 4

Sheet 4 includes the external footswitch inputs, front panel LED/Switch matrix, and control register (U11).

### Footswitch

The footswitch jack (J2) uses resistors (R10, R12) and capacitors (C8, C9) to filter out RFI. D10 and D11 help protect from over voltage or static shock and R11 and R13 provide a default non-active switch state of logic high.

### LED/Switch Matrix

Eight discrete front panel LEDs are organized into 2 columns and 4 rows.

An octal D-Flop U11 clocks the data bus on the rising edge of CTL_REG/. Bits 4 (COLUMN_STRB0) and 5 (COLUMN_STRB1) are active low column select lines which are buffered and inverted by switching transistors Q3 and Q4. When a selected COLUMN line is driven high and ROW line is driven low, the LED at the crosspoint of the column and row will light. Also, if the one of the front panel switches in the selected column is pressed, the SWITCH_ROW signal corresponding to its row will go high. R6 and R8 pull non-selected columns to ground for proper detection of the switches.

Row lines are driven directly from U11. As U11 is only driving four lines, total current in the IC remains well below 100 mA. The100Ω resistors (R70-R73) limit the row current to 28 mA or less.

## Sheet 5

Sheet 5 includes the power supply & master reset circuitry, the Midi I/O, S/PDIF output, and Z80 reset.

### Power Fail/Reset

Reset signaling is controlled by the +5UNREG voltage. If the +5UNREG voltage at the input of the +5VD regulator (U1) is high enough to create a 2 volt or greater drop across the regulator, then the differential between the voltage divider (R2 and R3 at the emitter of Q2, and the regulated +5VD at the base of Q2 will be enough to turn on Q2. As Q2 turns on, it charges C7 through R4. The voltage across R5 and R4 goes from 0V to about +6V. R4 is also used as a voltage divider to generate RESET/ at a 5V level taking Lexichip 3, CS5335 A/D, and the CNT_REG/ out of reset. C7 is discharged through D5 on power down.

The MPX 100 power supply provides three regulated DC output voltages: +5VD for digital circuits, +5VA and -5VA for analog circuits.

AC power is provided by an external transformer rated at 9VAC @1.9A. The transformer output is terminated with a 5mm/2.5mm barrel-type connector (J1), with its mating input jack located at the rear panel of MPX 100. A .1uF capacitor (C1) is connected across the AC input to help prevent noise spikes from entering the unit. In addition, C1 and C2 (470pf) prevent circuit-generated RFI from radiating through the power line.

All three regulated supplies (+5VDC analog, -5VDC analog and +5VDC digital) consist of a single diode (D1, D2 and D3) used as a half-wave rectifier to produce the unregulated 5 volt supply (approximately 10VDC) across each supply's filter capacitor (C3, C4, and C5). The analog supplies use 1000uF electrolytics. The digital supply uses a 3300uF electrolytic capacitor to handle the added load of more circuitry and front panel LEDs. Digital supply is post-regulator filtered with a 22 uF capacitor (C6) and analog circuit supplies use a 4.7uF, capacitor (C46) and a 22uF capacitor (C45). The +5VUNREG supply is monitored by the reset circuit for power up and power fail conditions.

Voltage regulation is handled by three TO-220 packaged ICs:

+5VD digital circuits - U1 (LM2490)
+5VA analog circuits - U14 (LM2490)
-5VA analog circuits - U15 (MC7905)

Current limiting and short circuit protection are incorporated into the internal circuitry of these ICs.

The MPX 100 power supply also provides two unregulated DC output voltages (+V and -V) for the analog output stage at U19. These power supplies help isolate the output stage from the rest of the power supply, and delay turn-on during power up to minimize power on thump characteristics at the analog output.

The unregulated +V supply (C99, C100, R132, R133 & Q6) and -V supply (C101, C102, R134, R135 & Q7) are both derived from capacitance multipliers which multiply the value of the capacitor by the beta of the transistor for higher output voltage.

Fifteen +5VD bypass caps are represented on page 5 of the schematic.

**MIDI I/O**

The MPX 100 MIDI interface complies with the MIDI specification. It incorporates 5-pin female DIN connectors for input and output (J4 and J3). MIDI IN is opto-coupled for ground isolation through U4 to the UART (in Lexichip 3). The MIDI OUT signal is provided by Lexichip 3 and is fed to current loop driver Q1 and out J3. FB1 and FB2 are used to reduce RFI radiation.

**S/PDIF Out**

The S/PDIF output signal is generated using a pair of 74HC132's. Each gate has to source about 6.25 mA, which is well within its capabilities. The resistors are selected so that the voltage across R52 is 0.5Vpp, assuming a 75Ω load resistor across the S/PDIF connector and a Voh out of the gates of 4.7V, with typical Voh at 6mA.

C28 and C30 band-limit the S/PDIF signal, but are necessary to meet RF compliance. D17 helps protect from over voltage or static shock.

**Z80 Reset**

In order to ensure that the data bus is tri-stated when the Lexichip 3 is released from reset, the Z80 requires a clock to be present at its ZCLK input when the Z80 is released. This is accomplished with a 74HC132 (U7), along with C32 (10pf) and R55 (47k) as a feedback oscillator. A 74HC157 (U6) is used to select the ZCLK source from either the U7 oscillator or the Lexichip 3, and to gate the reset signal for the Z80 during reset.

During power up, while RESET/ is asserted low, the feedback oscillator is enabled by bringing U7 pin 1 high. The oscillator output is selected as the ZCLK, and ZRST is held low by U6.

When the RESET/ signal goes high, the feedback oscillator is disabled as U7 pin 1 is brought low, the ZCLK_LEXI3 clock (from the Lexichip 3) signal is selected as the ZCLK, and ZRST is controlled by ZRST_LEXI3 signal (from the Lexichip 3).

## MAIN BOARD

| PART NO. | DESCRIPTION | QTY | EFF•INACT | REFERENCE |
|---|---|---|---|---|
| 200-11946 | POT,RTY,10KBX2,7MMFL,14,15L | 3 | | R81,87,105 |
| 200-12169 | POT,RTY,5K15AX2,7MMFL,14,15L | 1 | | R116 |
| 200-12184 | POT,RTY,10K15AX2,7MMFL,14,15L | 1 | | R97 |
| 202-09794 | RESSM,RO,5%,1/10W,0 OHM | 2 | •04/07/98 | R42,74 |
| 202-09794 | RESSM,RO,5%,1/10W,0 OHM | 3 | 04/07/98• | R42,74,127 |
| 202-09795 | RESSM,RO,5%,1/10W,2.2K OHM | 3 | | R15,31,32 |
| 202-09871 | RESSM,RO,5%,1/10W,1K OHM | 3 | | R6,8,83 |
| 202-09873 | RESSM,RO,5%,1/10W,10K OHM | 20 | •04/07/98 | R17,41,56-69,76-79 |
| 202-09873 | RESSM,RO,5%,1/10W,10K OHM | 24 | 04/07/98• | R17,41,56-69,76-79 R128-131 |
| 202-09894 | RESSM,RO,5%,1/10W,1M OHM | 1 | | R47 |
| 202-09897 | RESSM,RO,5%,1/10W,470 0HM | 2 | 04/07/98• | R132,134 |
| 202-09899 | RESSM,RO,5%,1/10W,47 OHM | 13 | | R18-30 |
| 202-10557 | RESSM,RO,5%,1/10W,4.7K OHM | 2 | | R10,12 |
| 202-10558 | RESSM,RO,5%,1/10W,47K OHM | 7 | | R11,13,48-51,55 |
| 202-10559 | RESSM,RO,5%,1/10W,100 OHM | 8 | | R33-36,44,100,111 R123 |
| 202-10569 | RESSM,RO,5%,1/10W,10 OHM | 1 | | R45 |
| 202-10586 | RESSM,RO,5%,1/4W,100 OHM | 2 | | R72,73 |
| 202-10892 | RESSM,RO,5%,1/10W,2K OHM | 2 | 04/07/98• | R133,135 |
| 202-11040 | RESSM,RO,5%,1/10W,150 OHM | 4 | | R106-109 |
| 202-11041 | RESSM,RO,5%,1/10W,680 OHM | 3 | | R7,9,37 |
| 202-11071 | RESSM,RO,5%,1/4W,75 OHM | 2 | | R88,98 |
| 202-11072 | RESSM,RO,5%,1/4W,220 0HM | 3 | | R14,16,38 |
| 202-11073 | RESSM,RO,5%,1/4W,270 OHM | 2 | | R39,71 |
| 202-11991 | RESSM,RO,5%,1/10W,2 OHM | 2 | | R86,99 |
| 202-12191 | RESSM,RO,5%,1/4W,330 OHM | 1 | | R70 |
| 202-12847 | RESSM,RO,5%,1/4W,2 OHM | 1 | •04/07/98 | R1 — '1206' size |
| 203-10424 | RESSM,RO,1%,1/10W,4.99K OHM | 2 | | R101,103 |
| 203-10578 | RESSM,RO,1%,1/10W,2.21K OHM | 1 | | R80 |
| 203-10583 | RESSM,RO,1%,1/10W,10.0K OHM | 6 | | R4,85,89,90,93,94 |
| 203-10840 | RESSM,RO,1%,1/10W,750 OHM | 2 | | R113,122 |
| 203-10895 | RESSM,RO,1%,1/10W,681 OHM | 1 | | R3 |
| 203-10896 | RESSM,RO,1%,1/10W,1.00K OHM | 1 | | R2 |
| 203-10897 | RESSM,RO,1%,1/10W,2.00K OHM | 4 | | R117-120 |
| 203-11075 | RESSM,RO,1%,1/10W,95.3 OHM | 1 | | R52 |
| 203-11079 | RESSM,RO,1%,1/10W,715 OHM | 2 | | R53,54 |
| 203-11083 | RESSM,RO,1%,1/10W,49.9K OHM | 1 | | R5 |
| 203-11519 | RESSM,THIN,1%,1.00M OHM,MELF | 2 | | R110,124 |
| 203-11734 | RESSM,RO,1%,1/10W,4.32K OHM | 2 | | R115,126 |
| 203-11996 | RESSM,RO,1%,1/10W,6.49K OHM | 1 | | R84 |
| 203-12167 | RESSM,RO,1%,1/10W,374 OHM | 2 | | R114,125 |
| 203-12198 | RESSM,RO,1%,1/10W,2.15K OHM | 2 | | R102,104 |
| 203-12199 | RESSM,RO,1%,1/10W,316 OHM | 2 | | R112,121 |
| 203-12248 | RESSM,RO,1%,1/10W,9.53K OHM | 2 | | R91,95 |
| 203-12249 | RESSM,RO,1%,1/10W,5.36K OHM | 2 | | R92,96 |
| 203-12478 | RESSM,RO,1%,1/10W,68.1K OHM | 1 | | R82 |
| 240-00609 | CAP,ELEC,10uF,16V,RAD | 14 | •04/07/98 | C7,24,48,49,53,59,62,63,76, C77,83,84,96,97 |
| 240-00609 | CAP,ELEC,10uF,16V,RAD | 16 | 04/07/98• | C7,24,48,49,53,59,62,63,76, C77,83,84,96,97,99,101 |
| 240-00614 | CAP,ELEC,47uF,16V,RAD | 2 | 04/07/98• | C100,102 |
| 240-06611 | CAP,ELEC,1000uF,25V,RAD | 1 | | C3 |

202-09734 Qty

| PART NO. | DESCRIPTION | QTY | EFF•INACT | REFERENCE |
|---|---|---|---|---|
| 240-06886 | CAP,ELEC,4.7uF,25V,AX | 1 | | C46 |
| 240-07695 | CAP,ELEC,1uF,50V,RAD | 3 | | C39,41,43 |
| 240-09541 | CAP,ELEC,3300uF,16V,RAD | 1 | | C5 |
| 240-12848 | CAP,ELEC,3300uF,16V,20%,RAD | 1 | | C4 |
| 241-00654 | CAP,TANT,22uF,16V,RAD | 2 | | C6,45 |
| 244-00661 | CAP,MYL,.047uF,5%,RAD,BOX | 2 | | C78,91 |
| 244-06883 | CAP,MYL,.01uF,5%,RAD | 1 | | C38 |
| 244-09390 | CAP,MYL,.01uF,5%,RAD,MINI | 2 | | C68,69 |
| 244-10423 | CAP,MYL,.22UF,10,RAD | 2 | | C74,85 |
| 245-09291 | CAPSM,CER,470pF,50V,NPO,5% | 3 | | C2,57,58 |
| 245-09875 | CAPSM,CER,.1uF,50V,Z5U,20% | 34 | | C1,12-21,27,29,31,33-37,44, C51,56,60,66,67,72,73,80,81, C88,89,93,94,98 |
| 245-09876 | CAPSM,CER,.01uF,50V,Z5U,20% | 2 | | C22,30 |
| 245-09895 | CAPSM,CER,10pF,50V,COG,10% | 3 | | C32,82,95 |
| 245-10561 | CAPSM,CER,100pF,50V,COG,5% | 4 | | C10,11,79,92 |
| 245-10562 | CAPSM,CER,150pF,50V,10% | 6 | | C8,9,47,61,75,86 |
| 245-10976 | CAPSM,CER,47pF,50V,NPO,5% | 5 | | C28,50,52,87,90 |
| 245-10977 | CAPSM,CER,330pF,50V,NPO,5% | 2 | | C54,55 |
| 245-11594 | CAPSM,CER,2200pF,50V,COG,5% | 2 | | C70,71 |
| 245-11625 | CAPSM,CER,33pF,50V,COG,5% | 2 | | C25,26 |
| 245-12485 | CAPSM,CER,.1uF,25V,Z5U,20% | 5 | | C23,40,42,64,65 |
| 270-11545 | FERRITESM,CHIP,600 OHM,0805 | 2 | | FB1,2 |
| 300-10509 | DIODESM,1N914,SOT23 | 12 | •04/07/98 | D5,6,8,12-16,18-21 |
| 300-10509 | DIODESM,1N914,SOT23 | 11 | 04/07/98• | D6,8,12-16,18-21 |
| 300-10563 | DIODESM,DUAL,SERIES,GP,SOT23 | 5 | •04/07/98 | D10,11,17,24,25 |
| 300-10563 | DIODESM,DUAL,SERIES,GP,SOT23 | 6 | 04/07/98• | D5,10,11,17,24,25 |
| 300-11599 | DIODESM,GP,1N4002,MELF | 4 | | D1-4 |
| 310-01007 | TRANSISTOR,2N3904 | 1 | 04/07/98• | Q6 |
| 310-01008 | TRANSISTOR,2N3906 | 1 | 04/07/98• | Q7 |
| 310-10422 | TRANSISTORSM,2N4403,SOT23 | 2 | | Q3,4 |
| 310-10510 | TRANSISTORSM,2N3904,SOT23 | 1 | | Q1 |
| 310-10565 | TRANSISTORSM,2N3906,SOT23 | 2 | | Q2,5 |
| 330-10535 | ICSM,DIGITAL,74AC273,SOIC | 1 | | U1 |
| 330-11990 | ICSM,LEXICHIP3B,100PIN,PQFP | 1 | | U5 |
| 330-12844 | ICSM,DIGITAL,74HC132,SOIC | 1 | | U7 |
| 330-12845 | ICSM,DIGITAL,74HC157,SOIC | 1 | | U6 |
| 340-10877 | ICSM,LIN,4556,DUAL OP AMP,SOIC | 1 | | U19 |
| 340-11573 | ICSM,LIN,NJM4580,DUALOPAMP,SOP | 4 | | U16,20-22 |
| 340-11576 | ICSM,LIN,7905,-5V REG,TO263 | 1 | | U15 |
| 340-11948 | ICSM,LIN,LM339,QUAD COMP,SOIC | 1 | | U12 |
| 340-12849 | ICSM,LIN,LM2940,5V REG,TO263 | 2 | | U1,14 |
| 346-10508 | ICSM,SS SWITCH,74HC4053,SOIC | 2 | | U18,23 |
| 350-10545 | ICSM,SRAM,8KX8,80NS,SOP,50uA | 1 | | U9 |
| 350-11919 | IC,ROM,27C010,MPX100,V1.9 | 1 | | U10 |
| 350-11940 | ICSM,EEPROM,24C04A,4K,SER,SOIC | 1 | | U2 |
| 350-12384 | ICSM,DRAM,1MX4,60NS,SOJ | 1 | | U3 |
| 355-11580 | ICSM,ADC,CS5335,20BIT,STER,SOP | 1 | | U17 |
| 355-11942 | ICSM,DAC,CS4327,20BIT,STR,SSOP | 1 | | U13 |
| 365-09883 | ICSM,uPROC,Z80,CMOS,10MHz,QFP | 1 | | U8 |
| 375-02247 | IC,OPTO-ISOLATOR,6N138 | 1 | | U4 |
| 390-09781 | CRYSTAL,11.2896MHz | 1 | | Y1 |
| 430-11938 | LED,T1,GRN,PCRA,BLOCK | 4 | | D7,9,22,23 |
| 430-11939 | LED,DUAL,T1,GRN/RED,PCRA,BLOCK | 2 | | D26,27 |
| 452-11947 | SW,RTY,ENC,16POS,4BIT,15.5L | 2 | | SW3,4 |
| 453-12165 | SW,PBM,1P1T,7MMSQ,250GF,PCRA | 3 | | SW1,2,5 |
| 510-06042 | CONN,DC POWER,PC,DJ005,2.5MM | 1 | | J1 |
| 510-09790 | CONN,DIN,5FC@180DEG,PCRA,SHLD | 2 | | J3,4 |
| 510-10555 | CONN,RCA,PCRA,1FCG,YEL | 1 | | J5 |
| 510-11087 | 1/4"PH JACK,PCRA,3C,SW-TR,G,FT | 2 | | J2,6 |

| PART NO. | DESCRIPTION | QTY | EFF•INACT | REFERENCE |
|---|---|---|---|---|
| 510-11548 | 1/4"PH JACK,PCRA,2C,SW-T,G,FT | 3 | | J7-9 |
| 520-09736 | IC,SCKT,32 PIN,PC,TIN,LO-PRO | 1 | | U10 |
| 704-12869 | HEATSINK,SMT,WING,3X.75",PSA | 1 | | U5 |
| 710-11910 | PC BD,MAIN,MPX100 | | | |

## CHASSIS/MECHANICAL PARTS

| PART NO. | DESCRIPTION | QTY | EFF•INACT | REFERENCE |
|---|---|---|---|---|
| 470-10162 | XFORMER,PLUG-IN,9VAC,1A,MSA-E | 1 | •04/13/98 | EURO ONLY |
| 470-12754 | XFORMER,PLUG-IN,120V,9VAC,1.9A | 1 | 04/13/98• | N.AMER ONLY |
| 470-12755 | XFORMER,PLUG-IN,230V,9VAC,1.9A | 1 | 04/13/98• | EURO ONLY |
| 470-12860 | XFORMER,PLUG-IN,120V,9VAC,1A | 1 | •04/13/98 | N.AMER ONLY |
| 550-11929 | KNOB,.69D,6MM/FL,BLK,LINE | 5 | | |
| 550-11930 | KNOB,.85D,6MM/FL,BLK,LINE | 2 | | |
| 550-11931 | BUTTON,.24X.64,BLK,W/LT PIPE | 3 | | |
| 635-12192 | SPCR,4-40X1/2,3/16HEX,AL | 1 | | PCB/BRKT TO FP |
| 640-02812 | SCRW,4-40X3/8,PNH,PH,BLK | 6 | 04/03/98• | CVR TO SIDE PAN (4); CVR TO FRONT PAN (2) |
| 641-10243 | SCRW,4-40X3/8,TH,T9,BZ,LOK | 6 | •04/03/98 | CVR TO SIDE PAN (4); CVR TO FRONT PAN(2) |
| 641-11834 | SCRW,TAP,AB,#2X1/4,PNH,PH,ZN | 2 | | DIN CONN |
| 650-03970 | POPRVT,1/8X1/8,REG PROT HD,SS | 1 | | BRACKET TO PCB |
| 700-11926 | COVER,MPX100 | 1 | | |
| 701-11934 | BRACKET,KEYSTONE,613,.147/.128 | 1 | | PCB TO FRONT PANEL |

# 6 Schematics

| | |
|---|---|
| 060-11918 | SCHEM,MAIN BD |
| | SCHEM,MASTER RESET CIRCUIT, REV 5 PC BOARD |
| | COMPONENT LAYOUT, MAIN BD |
| 080-11936 | ASSY DWG,CHASSIS |